

the input circuit comprises a decoder arranged to receive data synchronously from a source and a buffer for transferring data from the decoder to the asynchronous bus; and

the output circuit comprises an encoder arranged to output data synchronously to a destination and a buffer for transferring data from the asynchronous bus to the encoder.

3. (Amended) An editing system as claimed in claim [1 or] 2, further comprising a sizing circuit for varying the number of lines between said first multiplicity and said second multiplicity in each frame as data is transferred to the output circuit.

4. (Amended) An editing system as claimed in [any preceding] claim 3, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.

5. (Amended) An editing system as claimed in [any preceding] claim 4, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.

6. (Amended) An editing system as claimed in claim 5, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.

7. (Amended) An editing system as claimed in [any preceding] claim 6, further comprising:

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9. (Amended) An editing system as claimed in claim 8, wherein said processor is arranged to edit data at a processed data rate substantially corresponding to 24 frames per second and 625 lines, and the output circuit is arranged to output data at an output data rate substantially corresponding to the processed data rate.

10. (Amended) An editing system as claimed in claim 8, wherein said processor is arranged to edit data at a processed data rate substantially corresponding to 24 frames per second and 625 lines, and the output circuit is arranged to output data at an output data rate substantially corresponding to 30 frames per second and 525 line.

11. (Amended) An editing system as claimed in claim 10, wherein said processor is arranged to extract frame data from the frame-random access store as pairs of interleaved fields

and to repeat the transfer of one field of each pair to the output circuit thereby causing the output circuit to output the edited sequence at said frame rate of 30 per second.

12. (Amended) An editing system as claimed in [any preceding] claim 11, wherein said edited sequence comprises image frames derived from a first initial sequence comprising frames at a first frame rate and first line rate and image frames derived from a second initial sequence comprising frames at a second frame rate and second line rate different than said first frame and line rates, and wherein said processor is arranged to process the data for each frame in the edited sequence to conform to a line and frame rate corresponding to said output data rate.

Please add claims 15-40 as follows:

--15. (New) An editing system as claimed in claim 1, further comprising a sizing circuit for varying the number of lines between said first multiplicity and said second multiplicity in each frame as data is transferred to the output circuit.--

--16. (New) An editing system as claimed in claim 15, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.--

--17. (New) An editing system as claimed in claim 16, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.--

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--20. (New) An editing system as claimed in claim 19, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.--

--21. (Amended) An editing system as claimed in claim 15, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.--

--22. (New) An editing system as claimed in claim 21, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.--

--23. (New) An editing system as claimed in claim 22, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.--

--24. (New) An editing system as claimed in claim 23, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.--

--25. (New) An editing system as claimed in claim 1, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.--

--26. (New) An editing system as claimed in claim 1, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.--

--27. (New) An editing system as claimed in claim 26, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.--

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--28. (New) An editing system as claimed in claim 27, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.--

--29. (New) An editing system as claimed in claim 28, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.--

--30. (New) An editing system as claimed in claim 1, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.--

--31. (New) An editing system as claimed in claim 30, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.--

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--32. (New) An editing system as claimed in claim 2, further comprising a monitor connected to receive data from the output circuit at said output data rate for display of said edited sequence thereon.--

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--33. (New) An editing system as claimed in claim 2, further comprising a linear store connected to receive data from the output circuit at said output data rate for storage of said edited sequence therein.--

--34. (New) An editing system as claimed in claim 33, wherein said linear store comprises a video tape recorder selectively operable to output stored data at either said first frame rate or said second frame rate.--

--35. (New) An editing system as claimed in claim 34, further comprising:

a user operable input device; and wherein the editing processor is connected to the frame-random access store and for processing data representing one or more image frames of one or more initial sequences in response to the user operable input device to produce processed data representing an processed, edited sequence, which processed data is stored in the frame-random access store.--

--36. (New) An editing system as claimed in claim 35, wherein said one or more initial sequences are captured at a frame rate of 24 per second and each frame comprises 625 image lines, and the input circuit is arranged to receive the data and transfer the same to the store at an input rate substantially corresponding to 25 frames per second and 625 lines.--